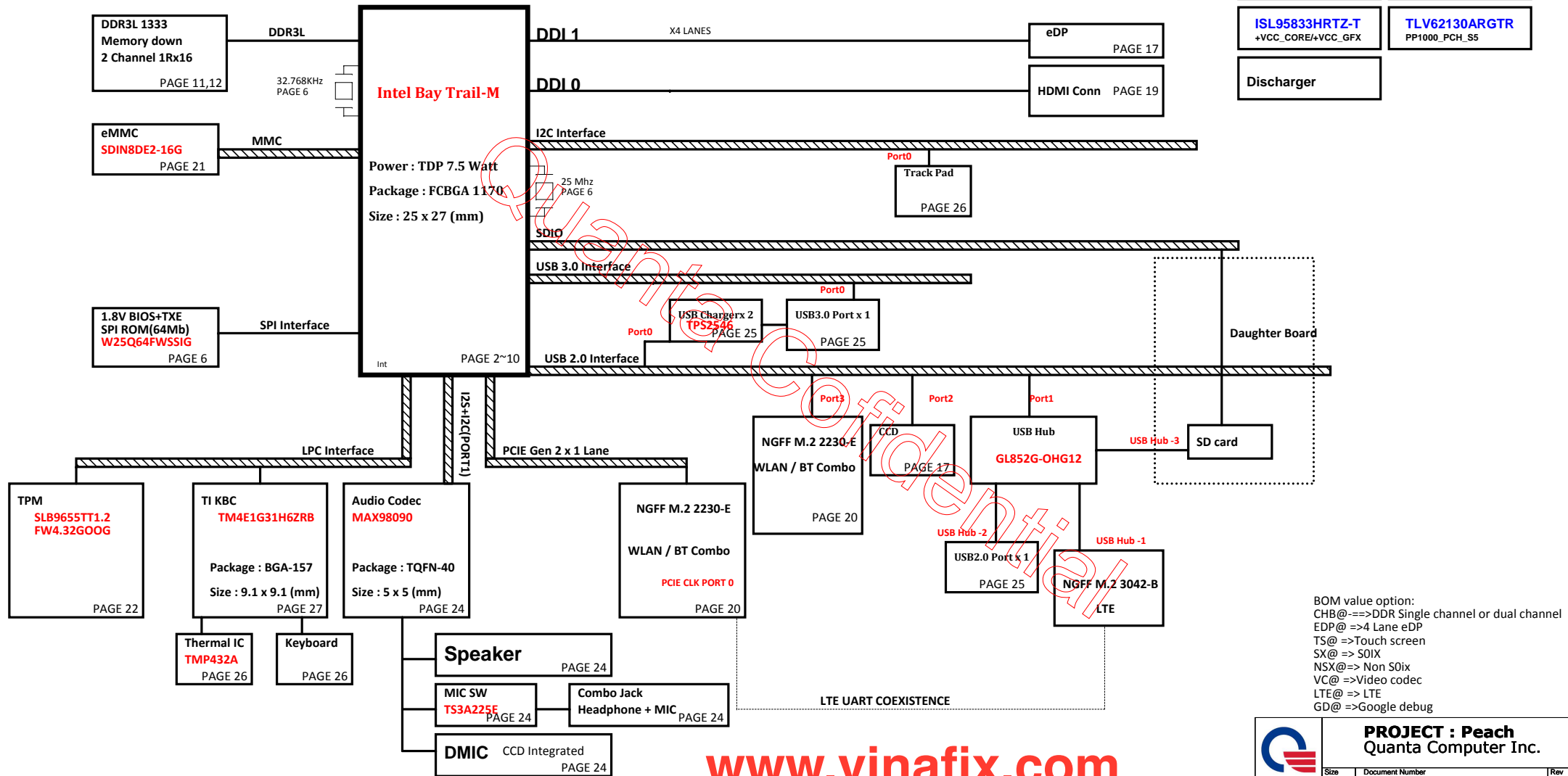


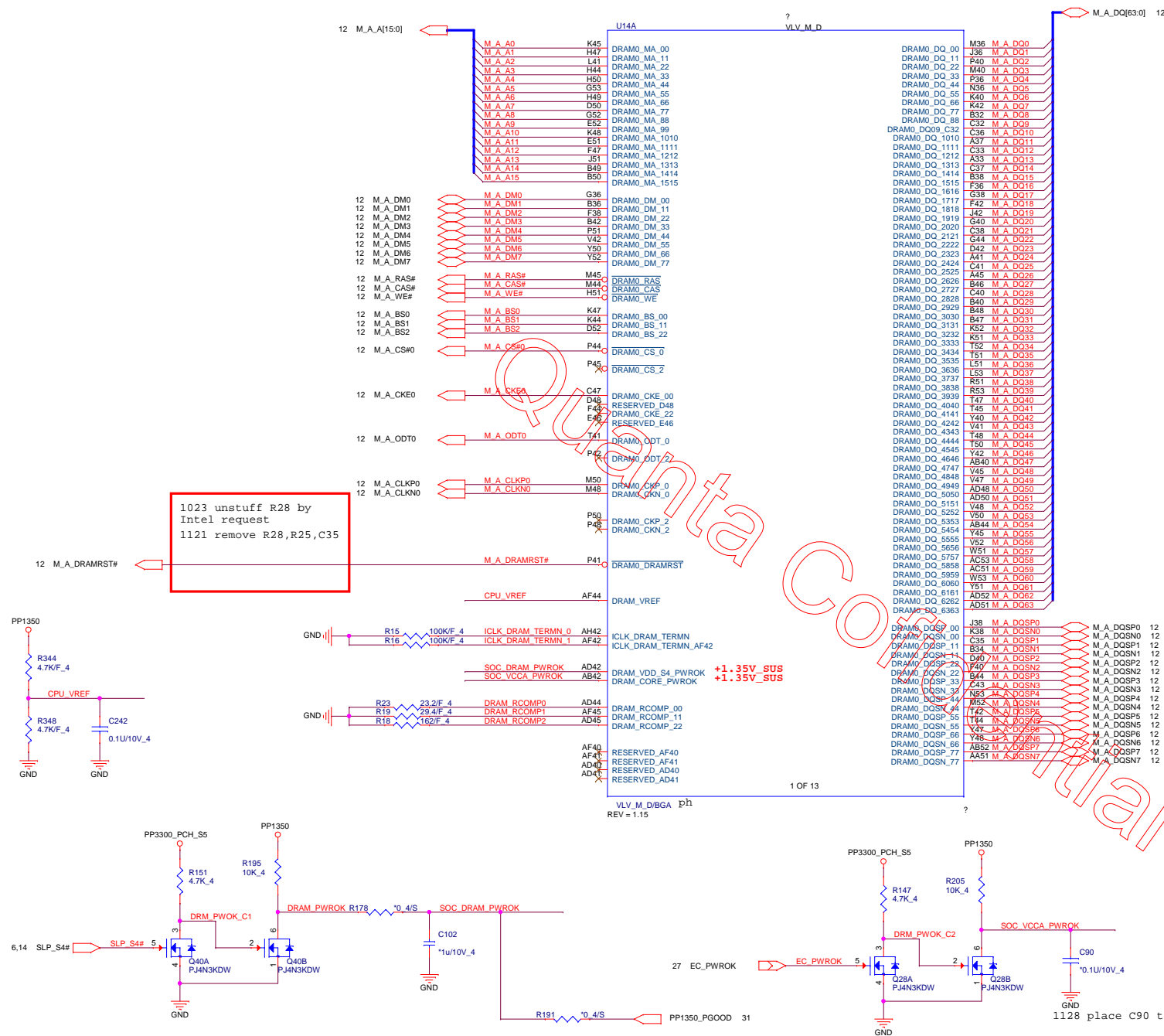
Intel Bay Trail-M Platform Block Diagram

SKUA QC N2920
AJ0QFW3UT05--CPU (1170P)N2920 1.86G QFW3(FCBGA)
SKUB DC N2820
AJ0QFW4UT02--CPU (1170P)N2820 2.13G QFW4(FCBGA)



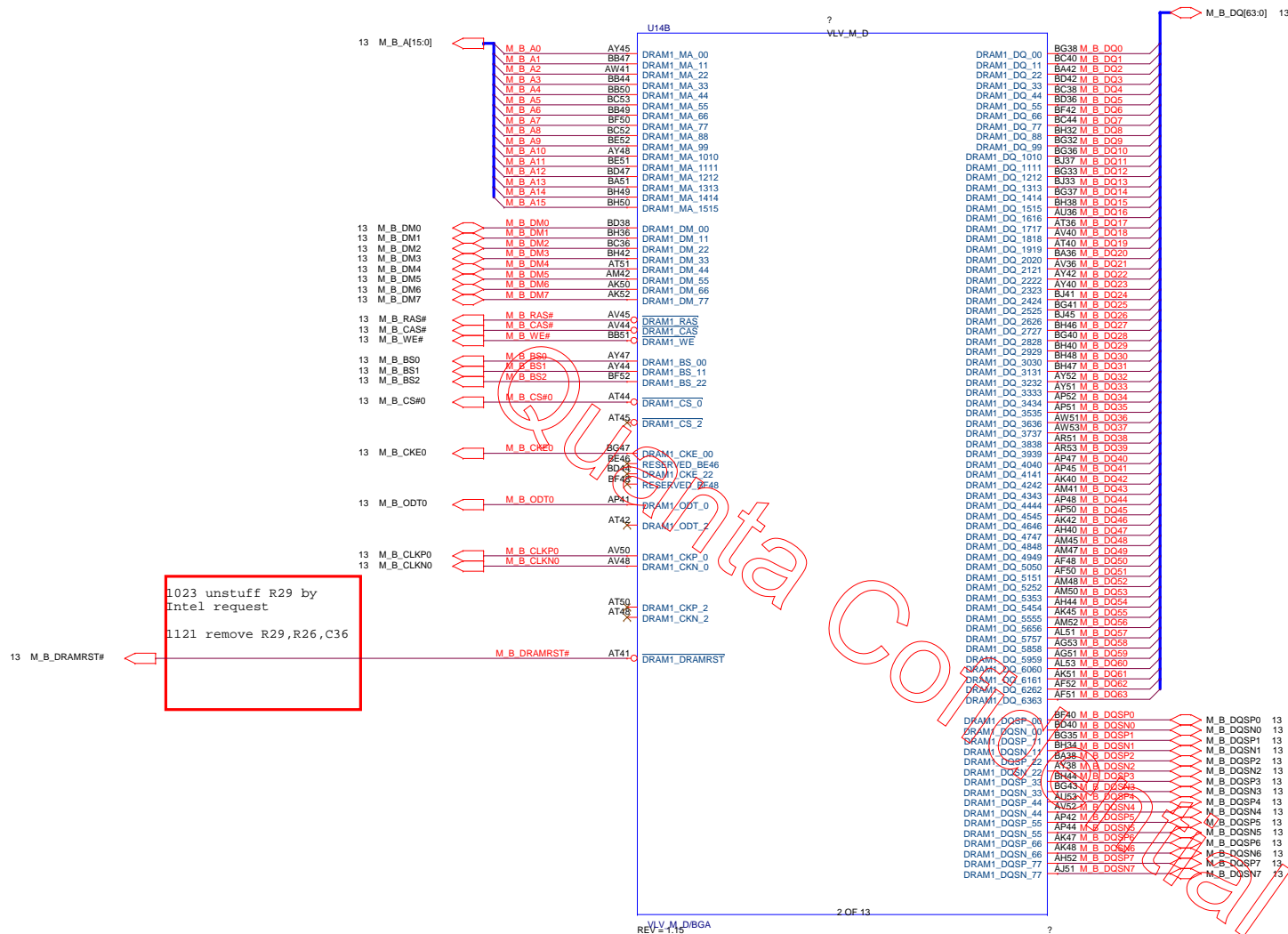
BOM value option:
CHB@ ==>DDR Single channel or dual channel
EDP@ ==>4 Lane eDP
TS@ ==>Touch screen
SX@ ==> S0IX
NSX@ ==> Non S0ix
VC@ ==>Video codec
LTE@ ==> LTE
GD@ ==>Google debug

www.vinafix.com

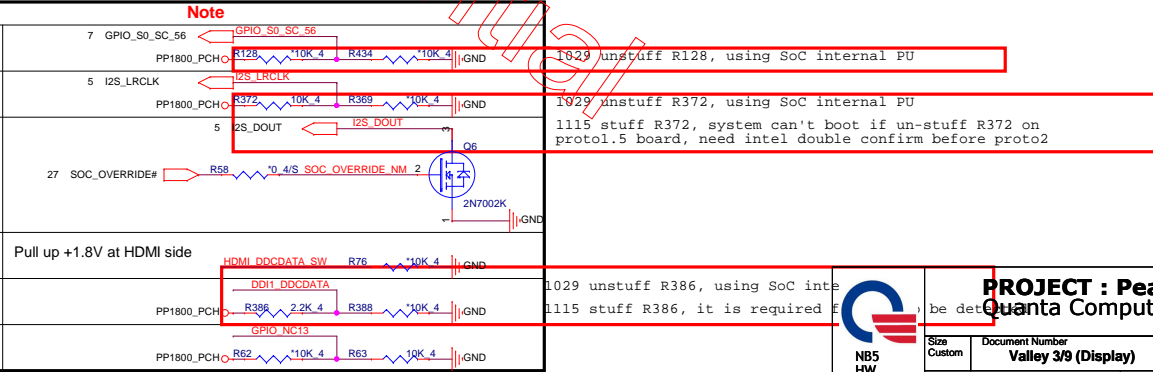


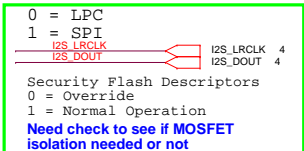
PROJECT : Peach
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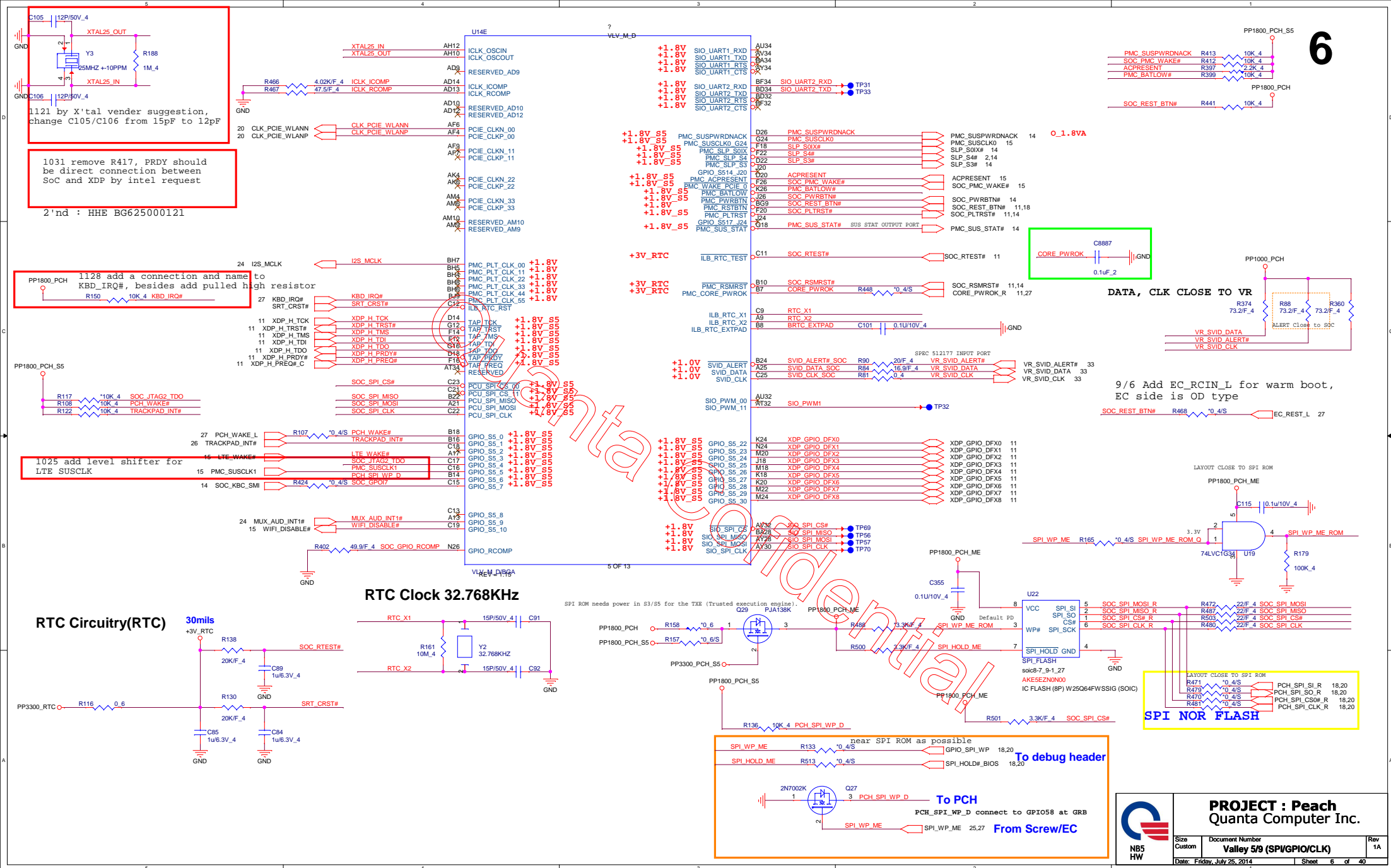
| | | |
|-----------------------------|-----------------------------------|--------|
| Size Custom | Document Number Valley 1/9 (DDR4) | Rev 1A |
| Date: Friday, July 25, 2014 | Sheet 2 of 40 | |



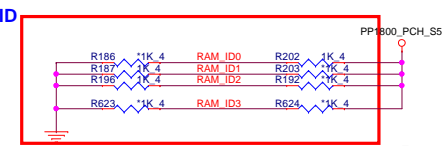
| Pin Name | Strap description | Sampled | Configuration | Note |
|---------------|----------------------------|---------|---|------|
| GPIO_SO_SC_56 | Top Swap (A16 Override) | PWROK | 0 = Top address bit is unchanged 1 = Top address bit is inverted | |
| LPE_I2S2_FRM | BIOS Boot Selection | PWROK | 0 = LPC 1 = SPI | |
| GPIO_SO_SC_65 | Security Flash Descriptors | PWROK | 0 = Override 1 = Normal operation | |
| DDI0_DDCDATA | DDI0 Detect | PWROK | 0 = DDI0 not detected 1 = DDI0 detected | |
| DDI1_DDCDATA | DDI1 Detect | PWROK | 0 = DDI0 not detected 1 = DDI0 detected | |
| GPIO_SO_NC_13 | | | | |







RAM ID



Freq. 1600MHz

| Vender | RAM_ID | Q PN | Mfr. PN | Channel | Size |
|--------|--------|-------------|----------------------|---------|------|
| Hynix | 001 | AKD5JGFTW11 | H5TC4G63AFR-PBA | 2CH | 4GB |
| Elpida | 000 | AKD5JGST410 | EDJ4216EFBG-GNL-F | 2CH | 4GB |
| Hynix | 011 | AKD5JGFTW14 | H5TC4G63AFR-PBR | 2CH | 4GB |
| Micron | 010 | AKD5DGSTL07 | MT41K128M16JT-125M:K | 2CH | 2GB |
| Elpida | 100 | AKD5JGST410 | EDJ4216EFBG-GNL-F | 1CH | 2GB |
| Hynix | 101 | AKD5JGFTW11 | H5TC4G63AFR-PBA | 1CH | 2GB |
| Hynix | 110 | AKD5JGFTW14 | H5TC4G63AFR-PBR | 1CH | 2GB |

C-test sku2

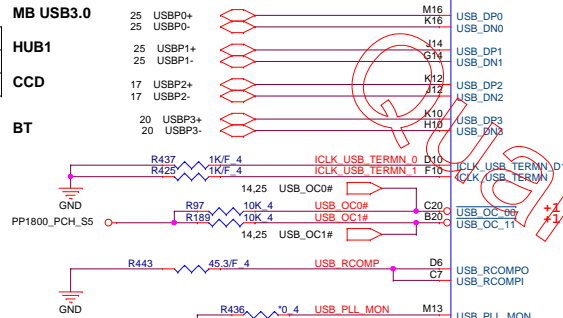
C-test sku4

C-test sku3

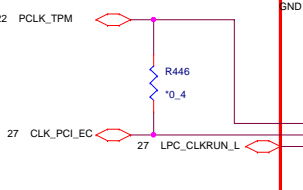
C-test sku1

PORT 1 USB CONN
PORT 2 LTE
PORT 3 CCD
PORT 4 BT

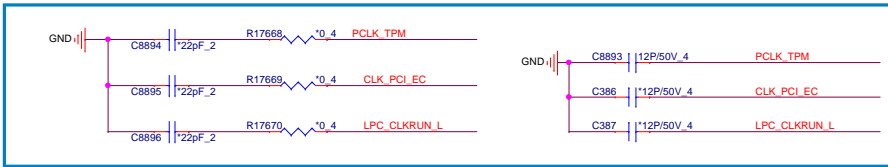
MB USB3.0
HUB1
CCD
BT



1101 add option BOM R446,R449 for EC CLK for power saving by Intel request



2014_0528_RF suggest



Un-Stuff for Test Only

Touch pad

Audio Codec

Light sensor(01/27 delete)

Touch panel(01/27 delete)



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| Size | Document Number | Rev |
|-----------------------------|--------------------------|-----|
| Custom | Valley 6/9 (USB/LPC/I2C) | 1A |
| Date: Friday, July 25, 2014 | Sheet 7 of 40 | |





<DDR>

BYTE2_16-23

BYTE3_24-31

BYTE1_0-7

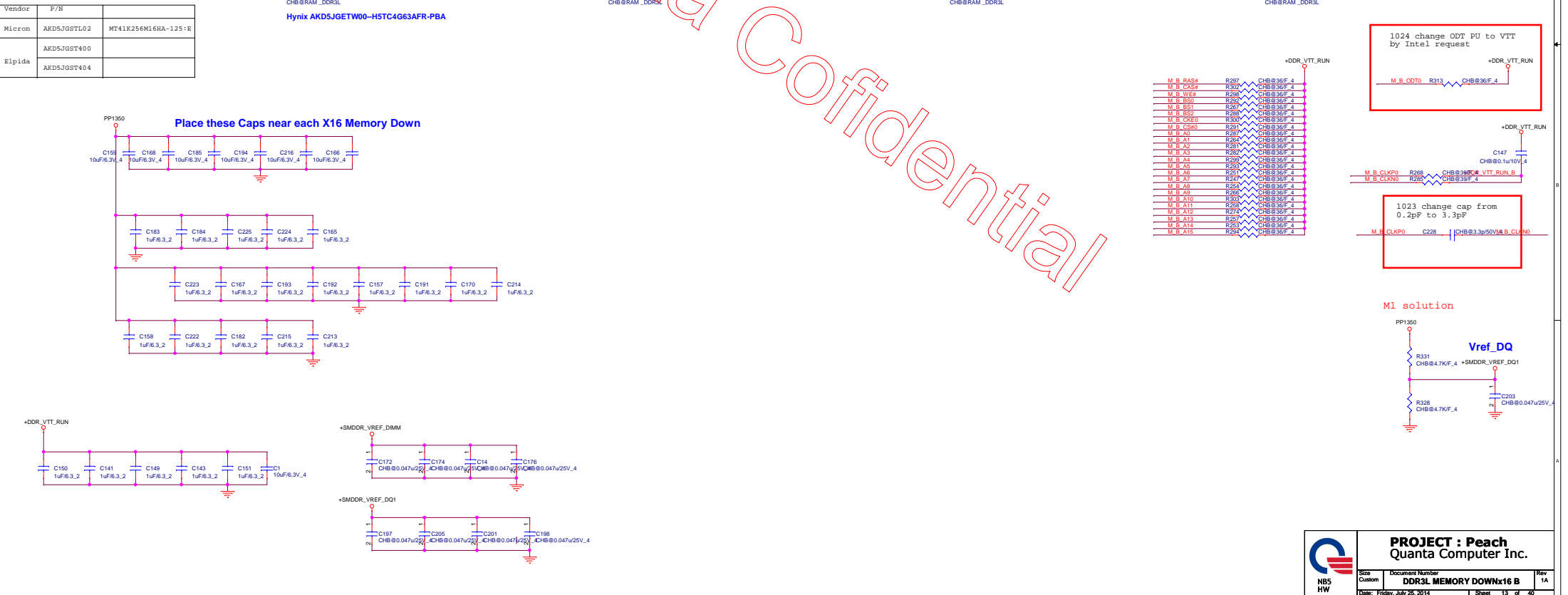
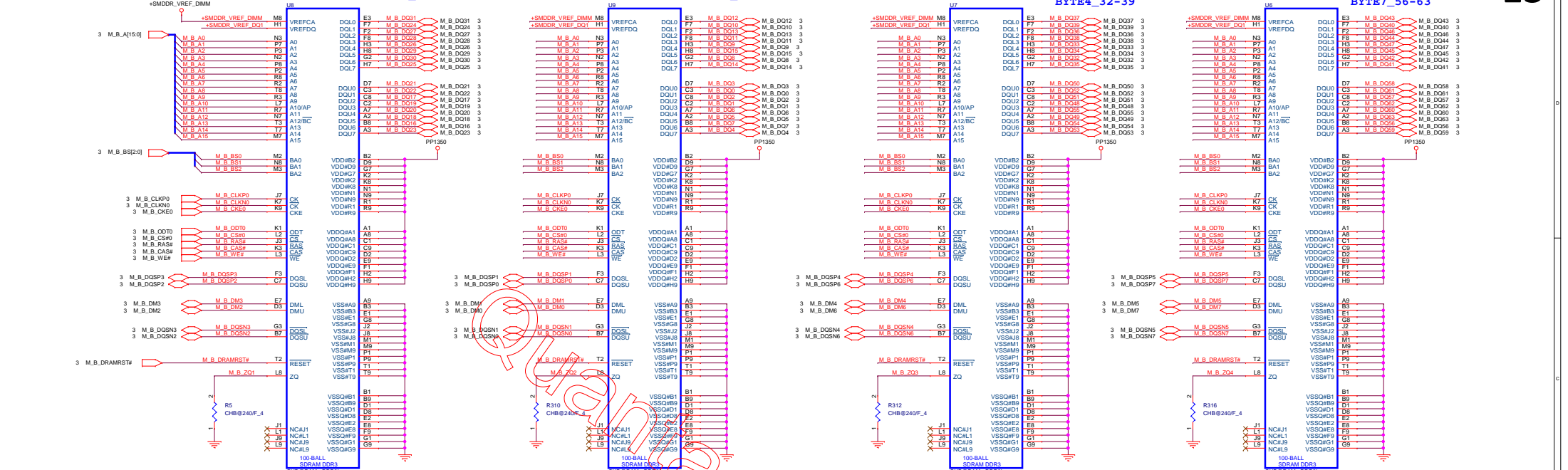
BYTE1_8-15

BYTE6_48-55

BYTE4_32-39

BYTE5_40-47

BYTE7_56-63



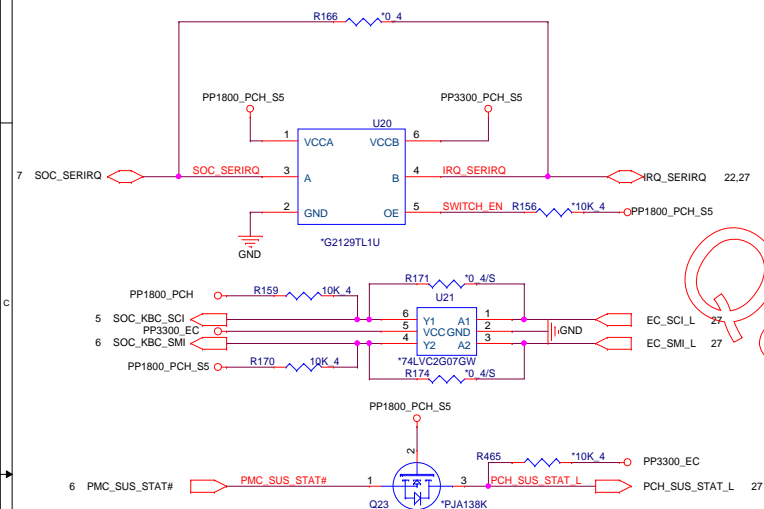
1024 change ODT PU to VTT by Intel request

1023 change cap from 0.2pF to 3.3pF

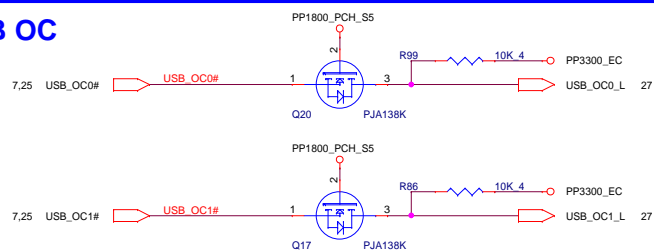
M1 solution

PWRON SEQUENCE

```
9/6 EC table says SERIRQ is OD pin, reserve for debugging
1128 remove R166, because SERIRQ of TPM needs 3V
1128 reserve 0 ohm R387/R391 on VCCA and VCCB for debugging
```

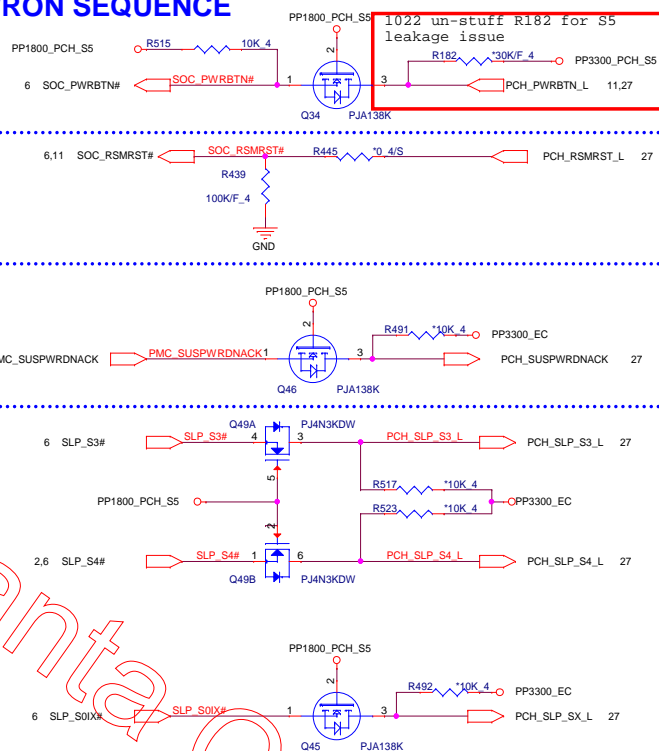


USB OC

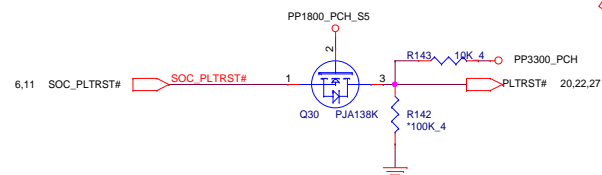


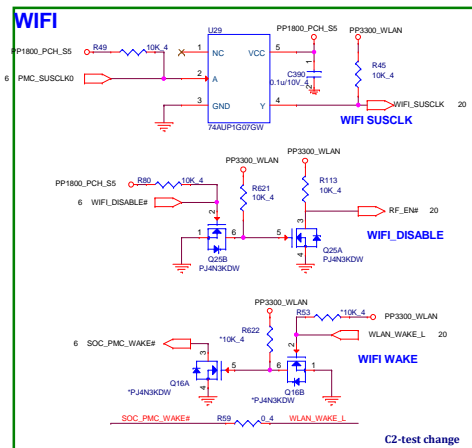
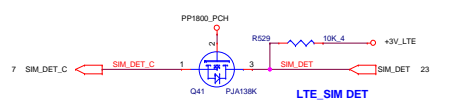
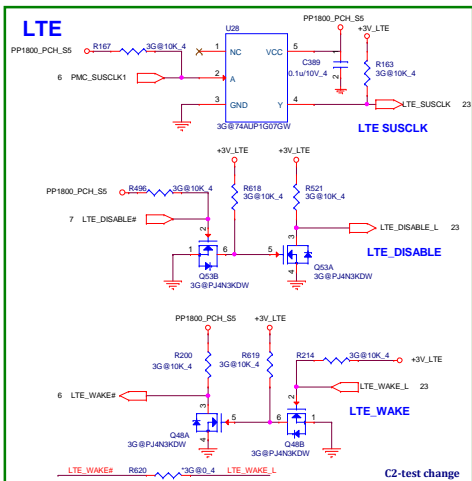
Stuffing for notifying EC

PWRON SEQUENCE

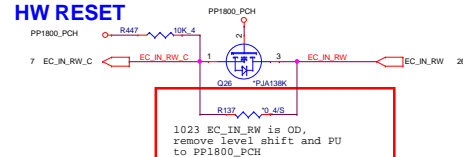


0220 remove SPI_SIO Interface,
Q35,Q36,Q37,Q44,R486,R484,R485,
R483,R426,R429,R427,R428





HW RESET



Touch Screen(01/27 delete)

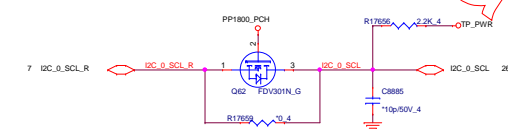
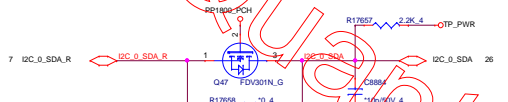
S0

S5

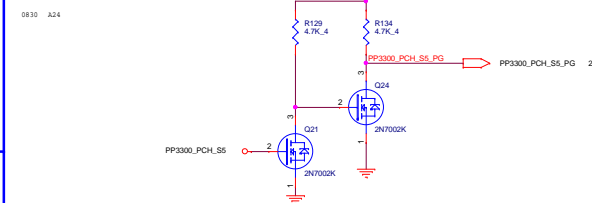
SATA

1025 Delete complete SSD(connector and caps)

Track Pad

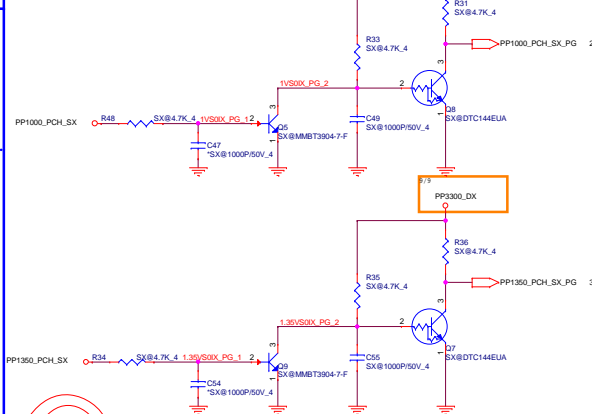


S5 Power Good(+3V_S5)



S0iX Power Good

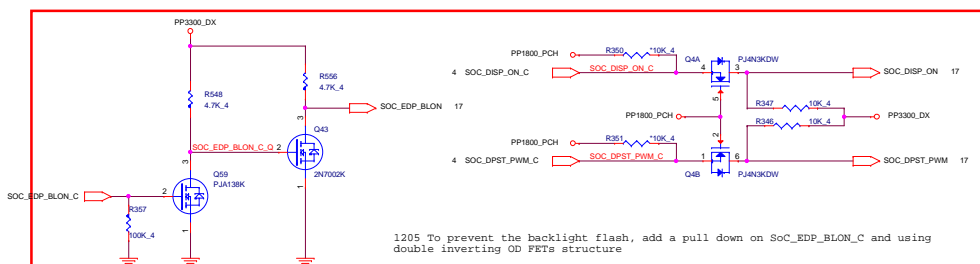
for proto type only, can remove at MP stage if S0ix is not needed

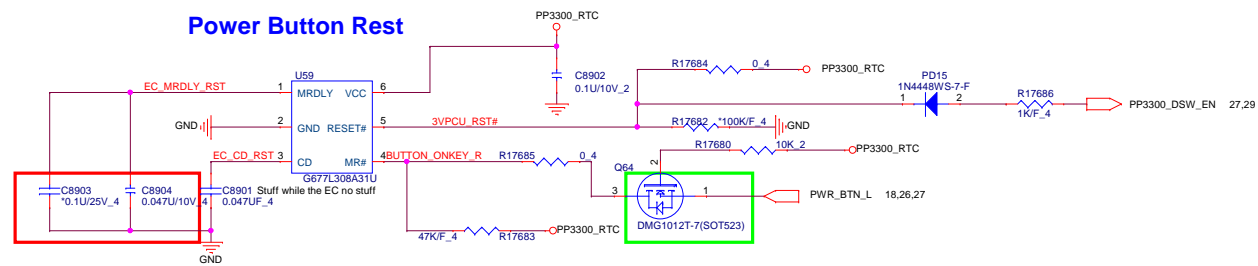


AC Detect



eDP control pin





Quanta Confidential

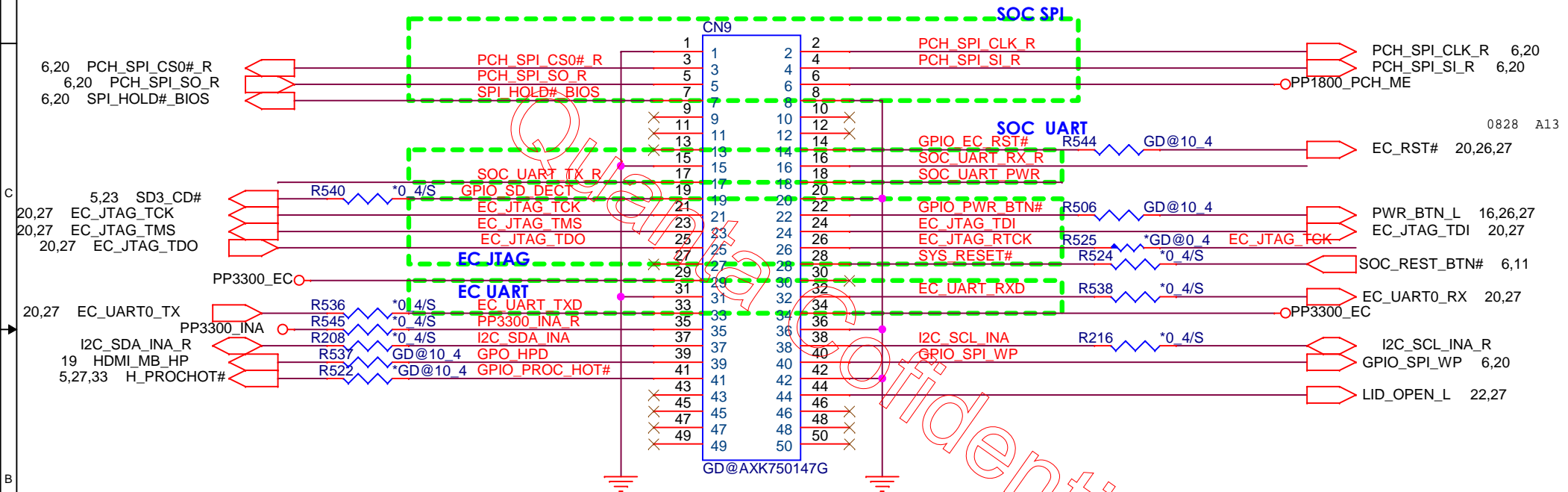
GOOGLE Debug Port(MPC)

50 pin BTB is **MUST**, don't use 42 pin

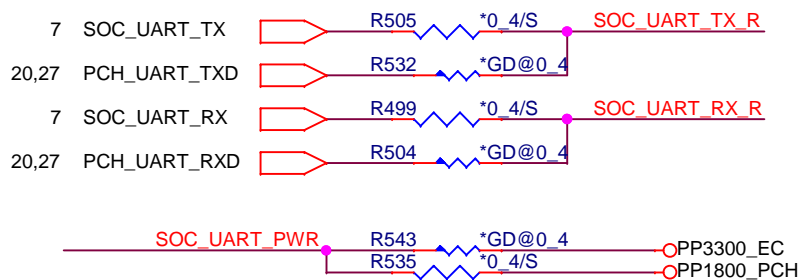
Socket part number AXK750147G

| | | | | | |
|-------|----|-------|----|-------|----|
| PIN7 | OD | PIN39 | OD | PIN49 | OD |
| PIN14 | OD | PIN41 | OD | PIN50 | OD |
| PIN19 | OD | PIN43 | OD | | |
| PIN22 | OD | PIN44 | OD | | |
| PIN28 | OD | PIN45 | OD | | |
| PIN30 | OD | PIN46 | OD | | |
| PIN37 | OD | PIN47 | OD | | |
| PIN38 | OD | PIN48 | OD | | |

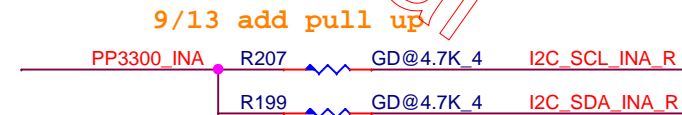
18



1021 change footprint and PN



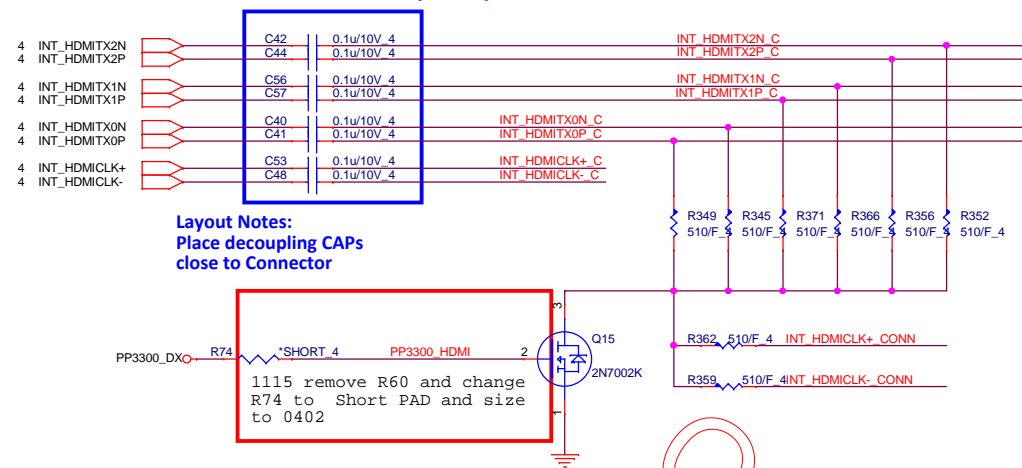
9/6 using optional instead of level shifted, default is from SoC



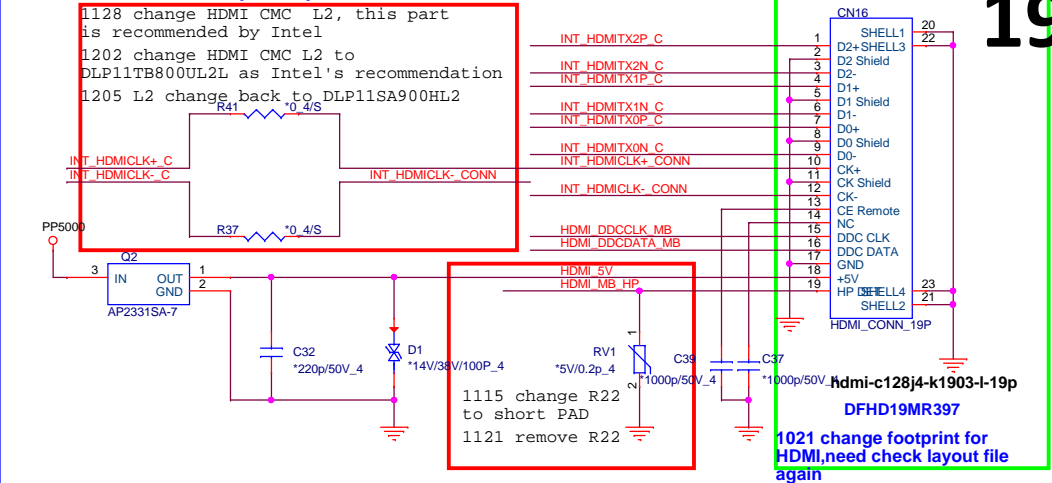
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| | | |
|-----------------------------|--|--------|
| Size Custom | Document Number Google Debug | Rev 1A |
| Date: Friday, July 25, 2014 | Sheet 18 of 40 | |

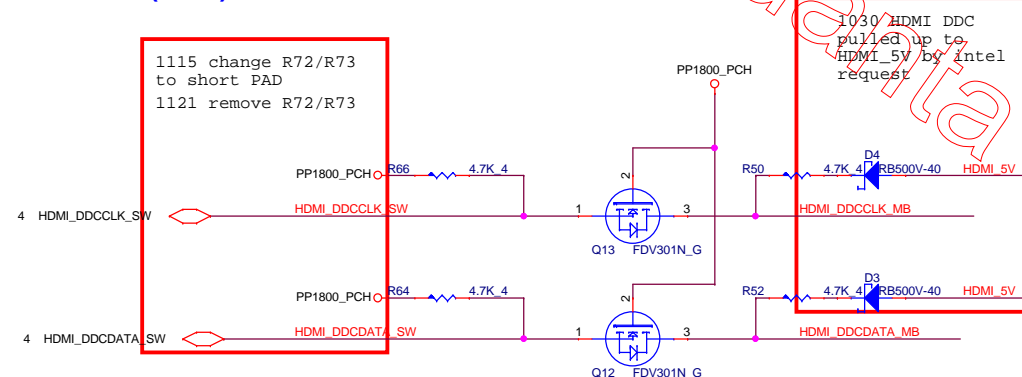
HDMI Cost Reduced level shift (HDM)



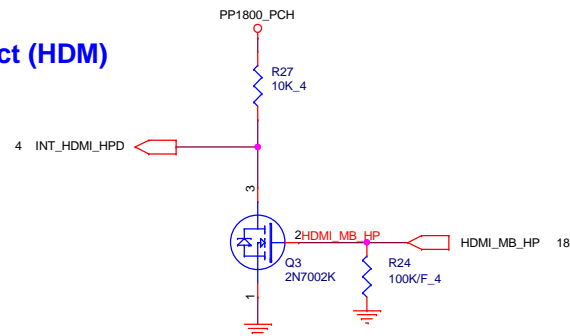
HDMI connector (HDM)



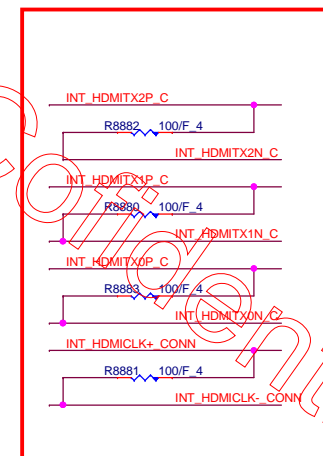
HDMI DDC (HDM)



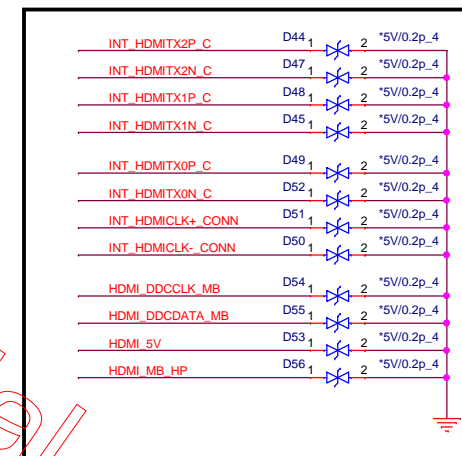
HDMI-detect (HDM)



EMI



ESD 靠近HDMI CONNECTOR(CN16)



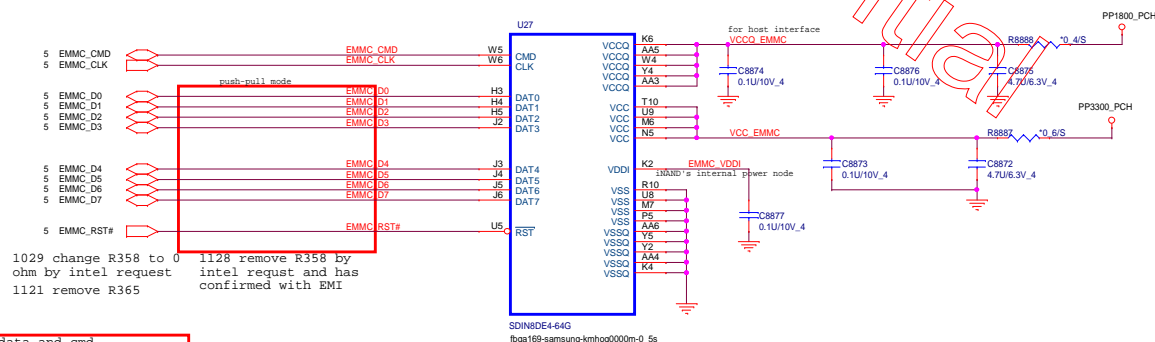
PROJECT : Peach
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| Size | Document Number | Rev |
|-----------------------------|-----------------|-----|
| Custom | HDMI | 1A |
| Date: Friday, July 25, 2014 | Sheet 19 of 40 | |



1025 Delete complete SSD(connector and caps)

EMMC (CBS)



| | |
|--|--|
| 1029 change R358 to 0 ohm by intel request | 1128 remove R358 by intel request and has confirmed with EMI |
| 1121 remove R365 | |

```
1029 remove pulled up resistors for eMMC data and cmd
1211 add back pulled up resistors
1212 all Pulled up resistors of eMMC data/cmd to be un-stuffed,
and R361 change to 47K ohm as well
```

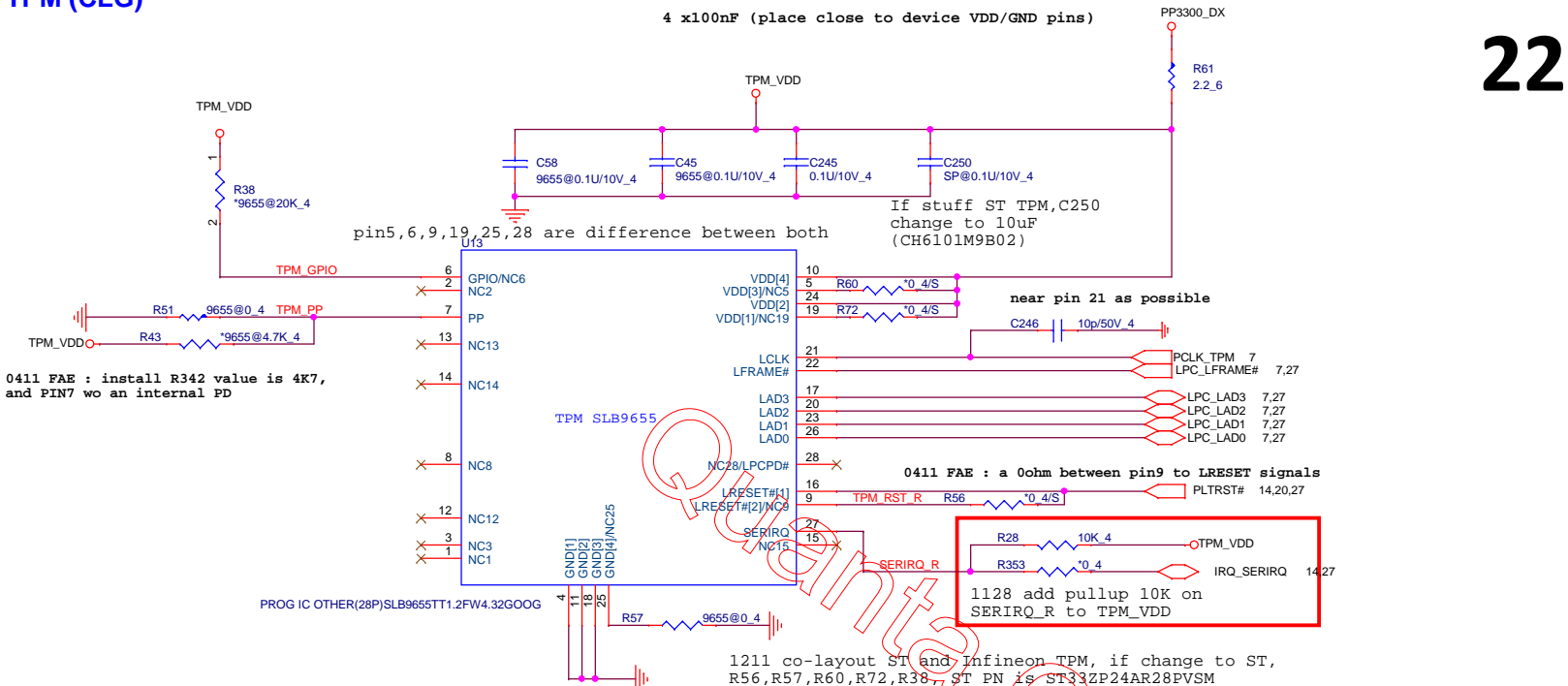
R361 change to 47K ohm as well

PP1800_PCH

| Component | Value | Signal |
|-----------|--------|----------|
| R396 | *47K 4 | EMMC D0 |
| R401 | *47K 4 | EMMC D1 |
| R469 | *47K 4 | EMMC D2 |
| R393 | *47K 4 | EMMC D3 |
| R406 | *47K 4 | EMMC D4 |
| R405 | *47K 4 | EMMC D5 |
| R404 | *47K 4 | EMMC D6 |
| R417 | *47K 4 | EMMC D7 |
| R361 | *47K 4 | EMMC CMD |

IC FLASH(153P) SDIN8DE4-64G(BGA)TOPBSQ

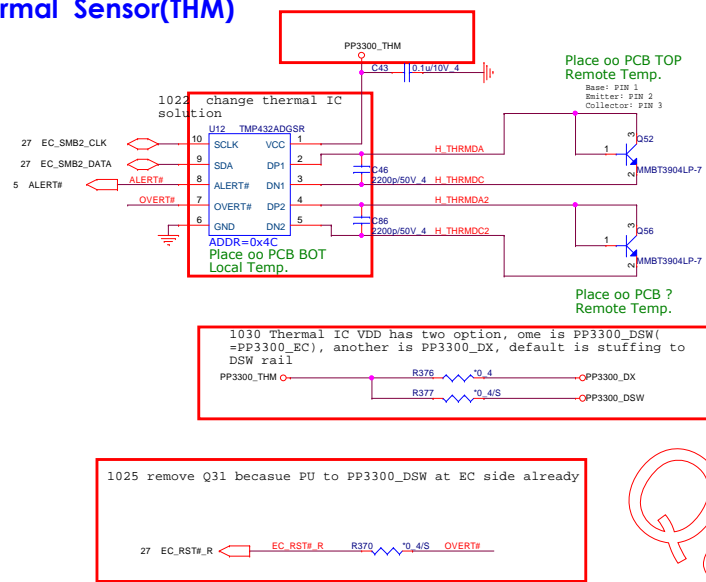
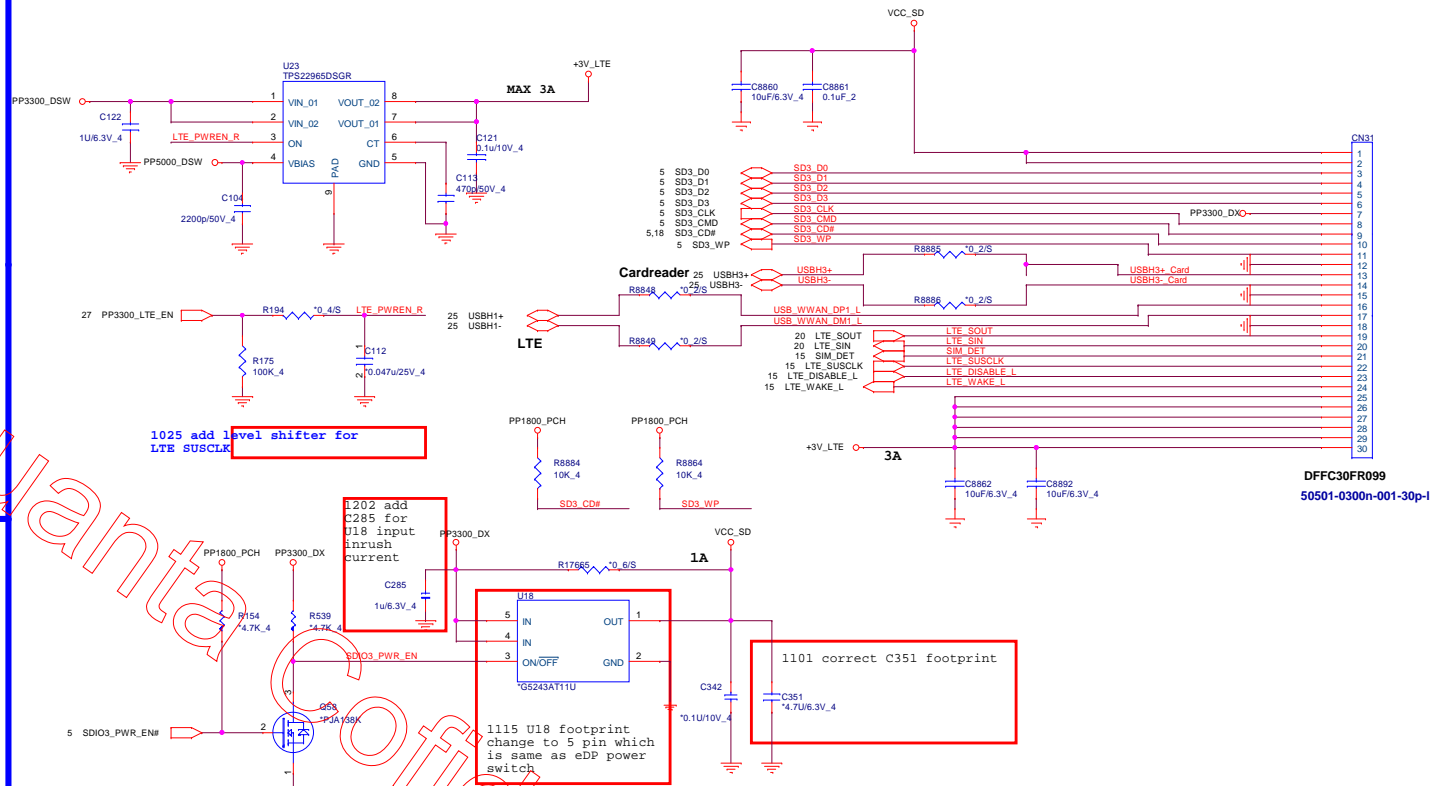
TPM (CLG)



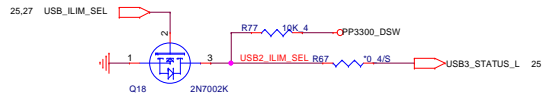
LED(UIF)

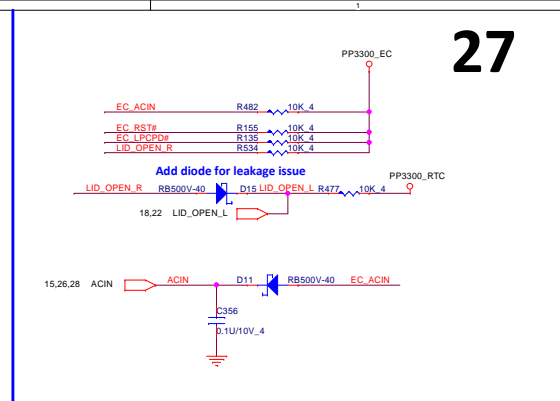


Thermal Sensor(THM)

FUNCTION DB
LTE(MNC)

USB Switch Current Control

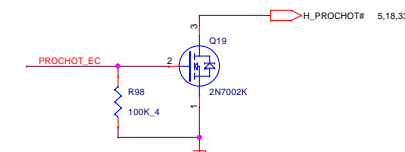
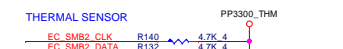




BATT and CHARGER / LCD BL PP3300_EC



1030 Thermal IC VDD has two option, one is PP3300_DSW(=PP3300_EC), another is PP3300_DX, default is stuffing to DSW rail



| | |
|----------|------------------|
| SM Bus 0 | BATT and CHARGER |
| SM Bus 1 | NA |
| SM Bus 2 | THERMAL SENSOR |
| | |

EC_REST_L
BAT_LED0
BAT_LED1
PCH_RSMRST_L
SMBUS
IRQ_SERIRQ
EC_BL_DISABLE_L

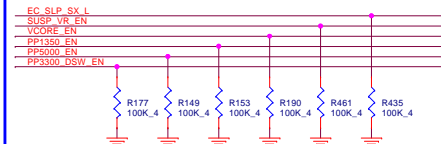
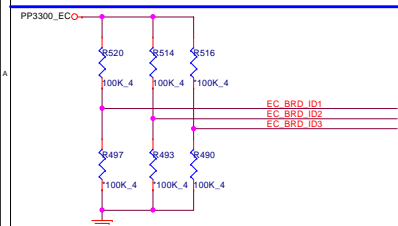
| | |
|--|--|
| | |
|--|--|



PROJECT : Peach
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| | | |
|-----------------------------|---|-----------|
| Size Custom | Document Number KBC TI TM4E1G31H6ZRBI | Rev 1A |
| Date: Friday, July 25, 2014 | Sheet 27 of 40 | |

| stage \ MB ID | EC_BRD_ID3 | EC_BRD_ID2 | EC_BRD_ID1 |
|---------------|------------|------------|------------|
| Proto | 0 | 0 | 0 |
| EVT | 0 | 0 | 1 |
| DVT | 0 | 1 | 0 |
| Ramp | 0 | 1 | 1 |

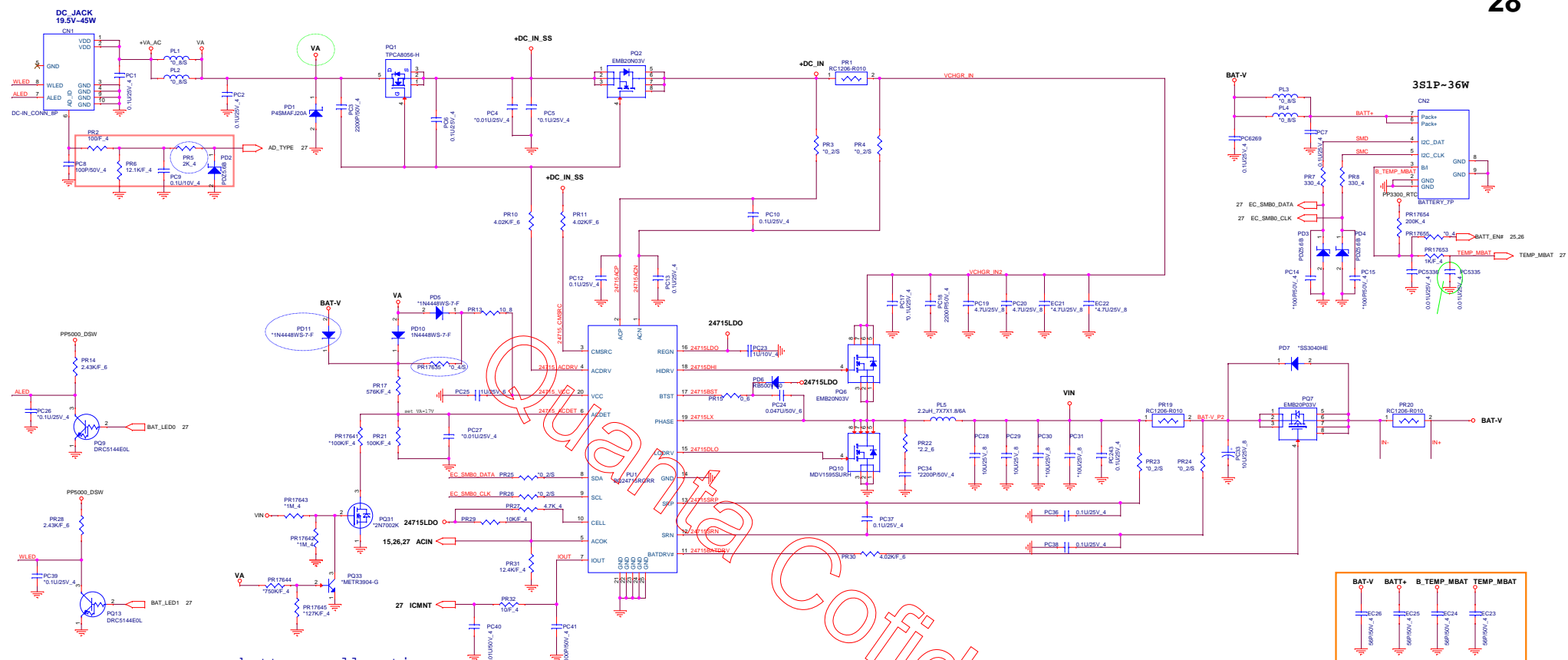


1211 add Test points on unused pins, need check layout to see if all points are ok

1212 change part number of EC ,which has a trial firmware inside

1121 by X'tal vender suggestion,
change C107/C109 from 15pF to 18pF

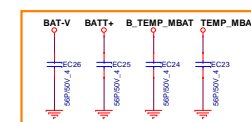
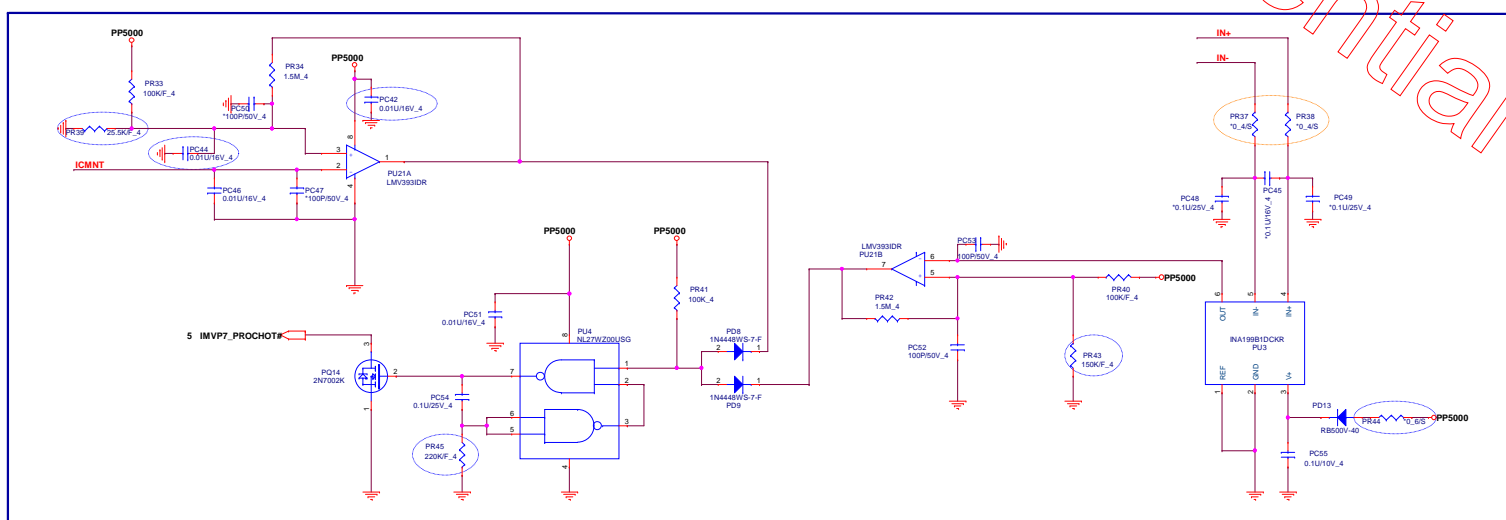
1121 by X'tal vender suggestion,
change C107/C109 from 15pF to 18pF



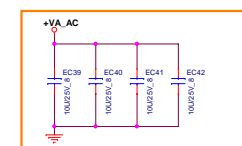
battery cell option

| | | |
|------|----------|--------|
| | 2-cell | 3-cell |
| PR27 | un-stuff | stuff |

10ms one-shot circuit

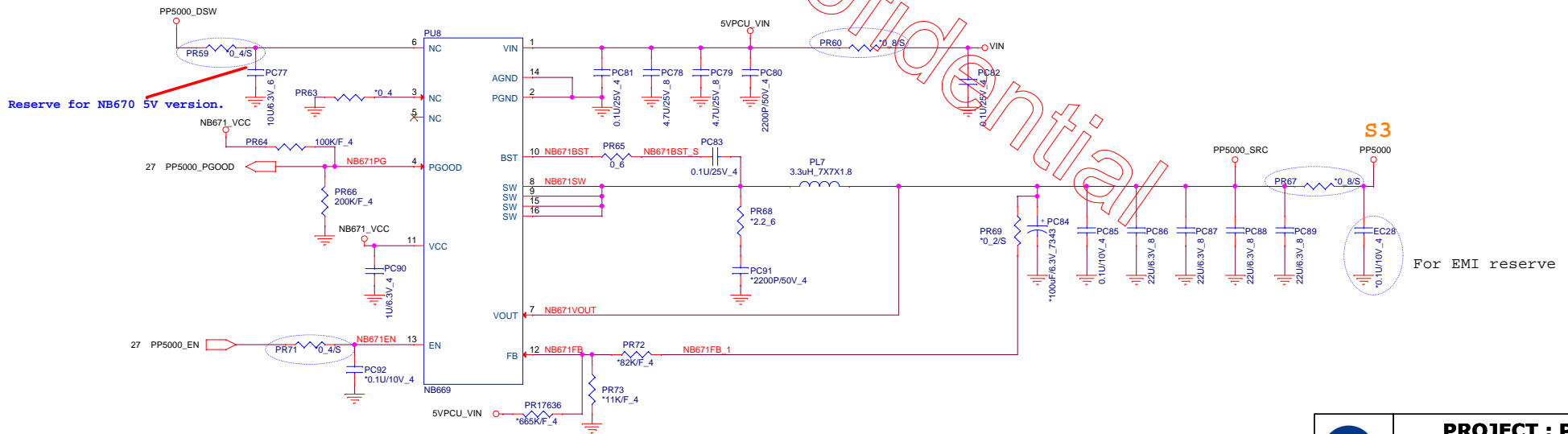
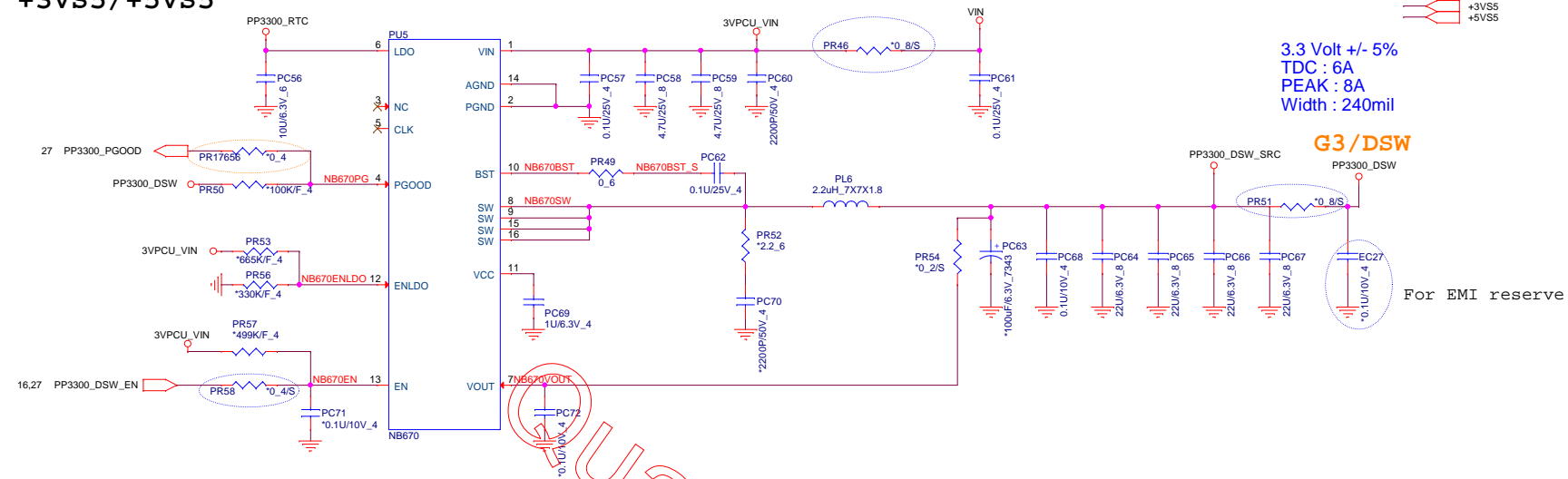


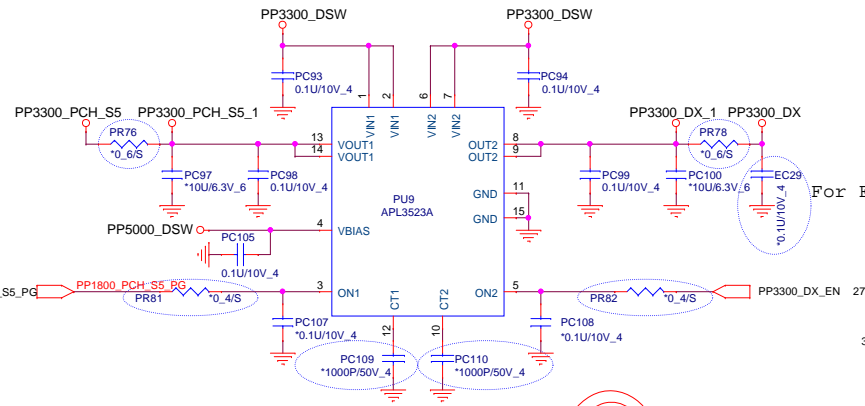
For EMI



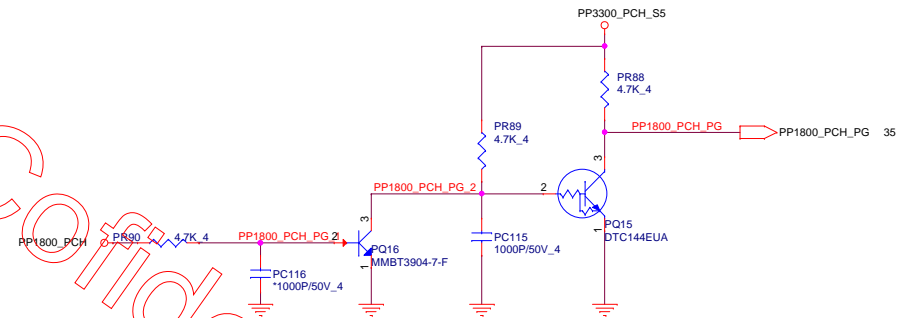
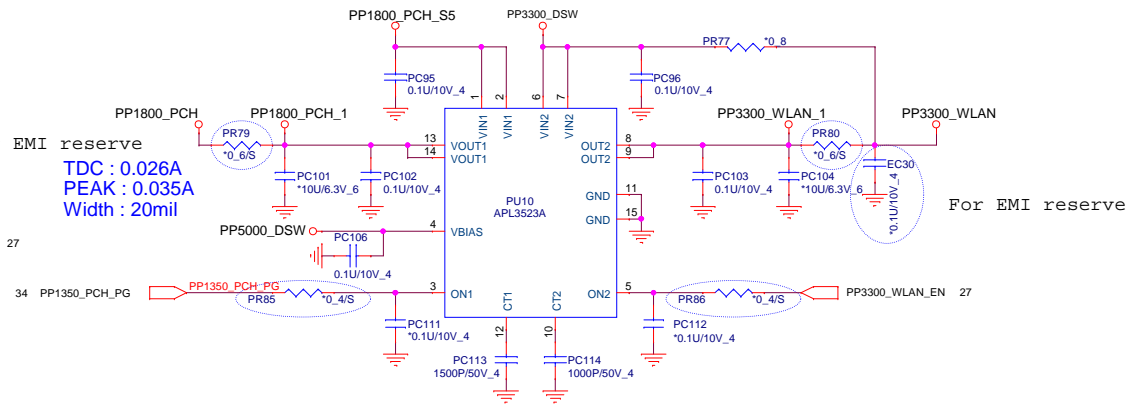
For EMI ISN

DC/DC +3VS5/+5VS5



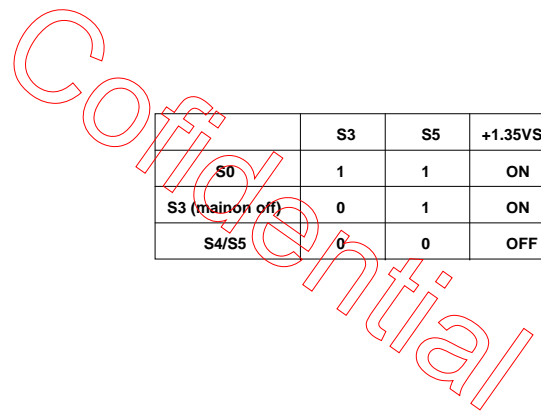


For EMI reserve
 TDC : 0.026A
 PEAK : 0.035A
 Width : 20mil

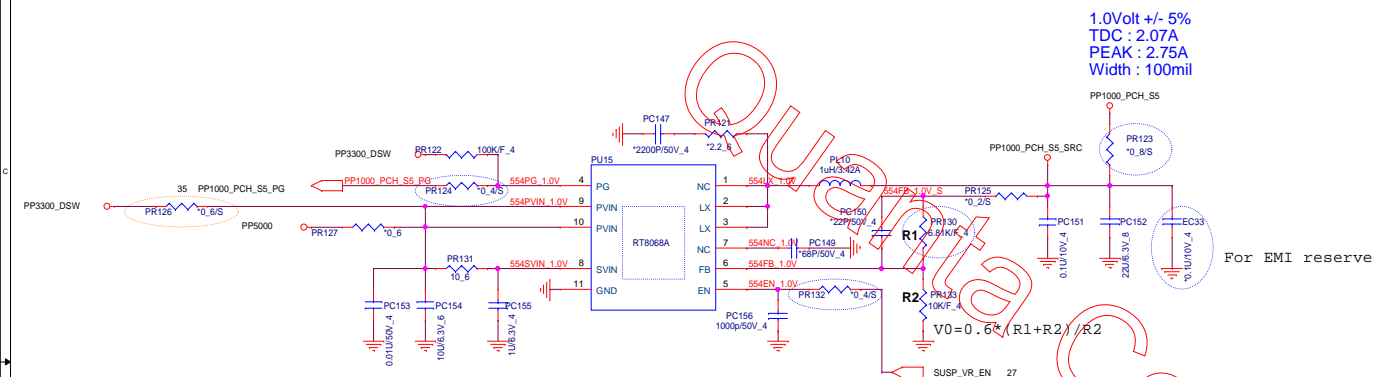
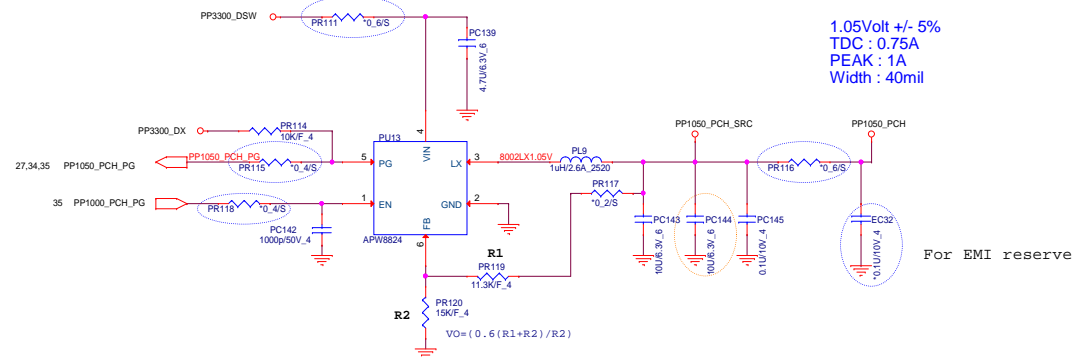


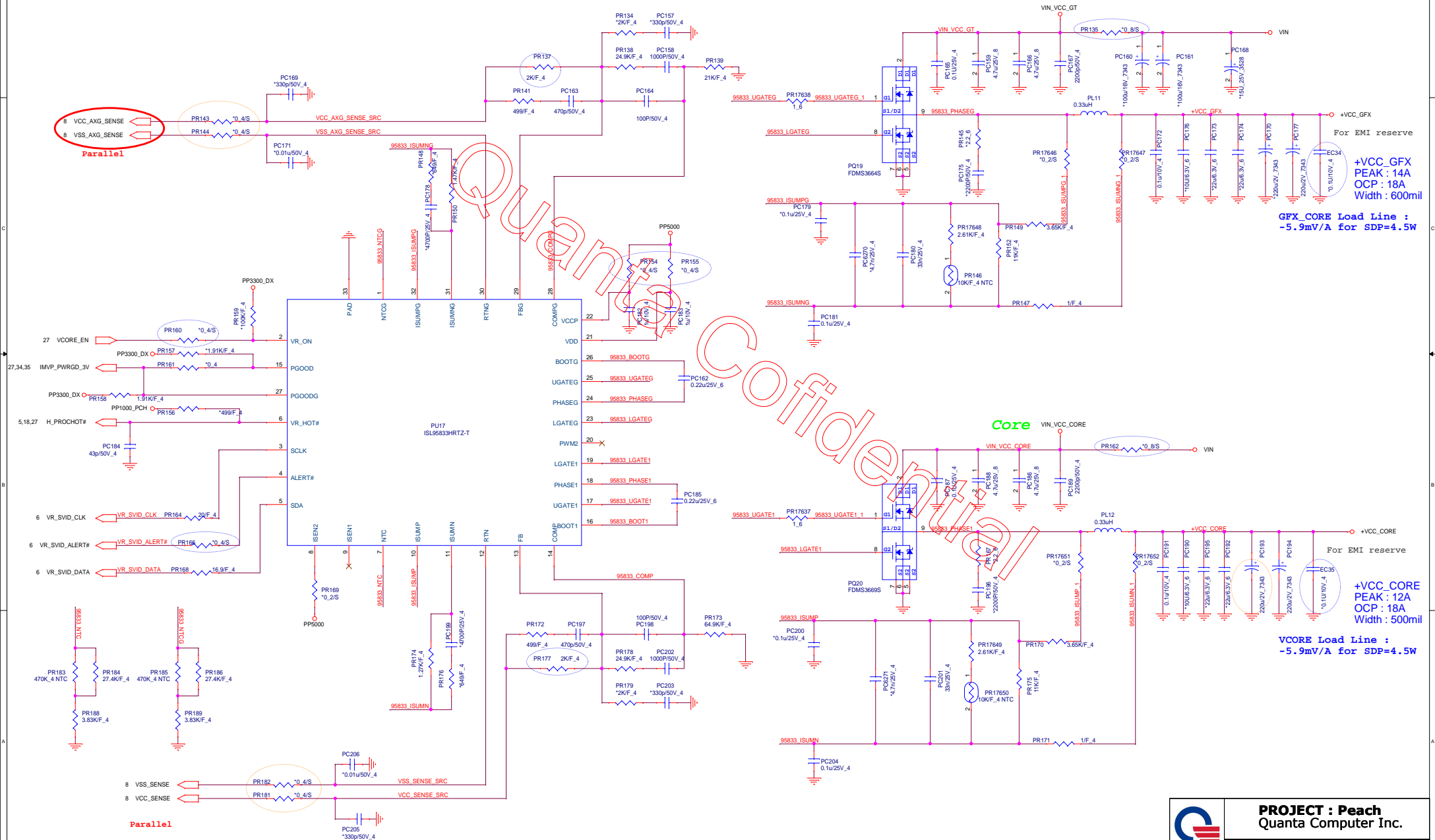
PROJECT : Peach
 Quanta Computer Inc.

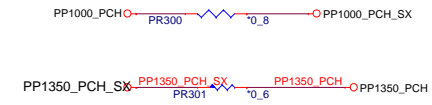
| Size | Document Number | Rev |
|-----------------------------|-----------------|-----|
| Custom | Load Switch | 1A |
| Date: Friday, July 25, 2014 | Sheet 30 of 40 | |

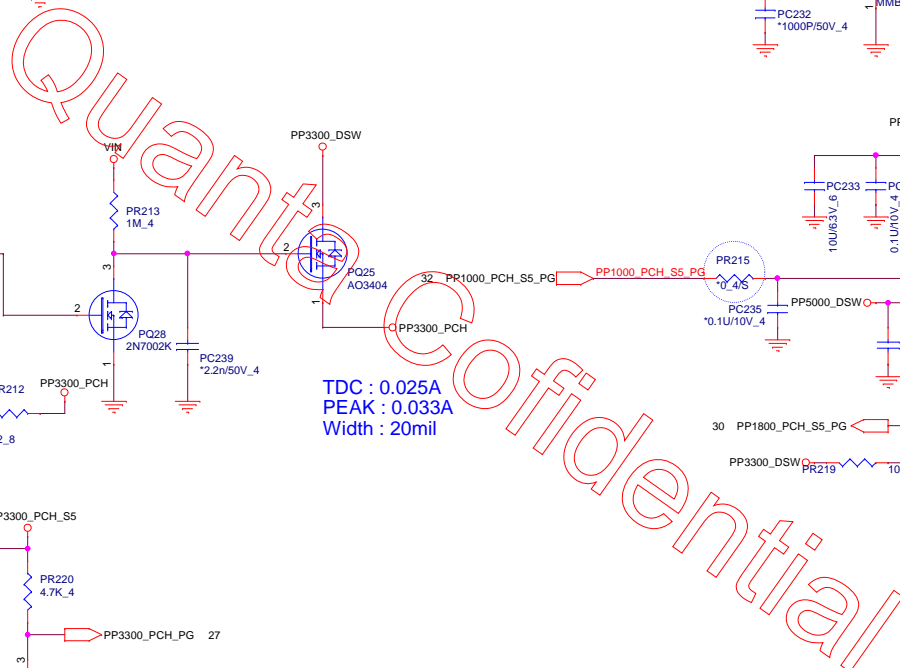


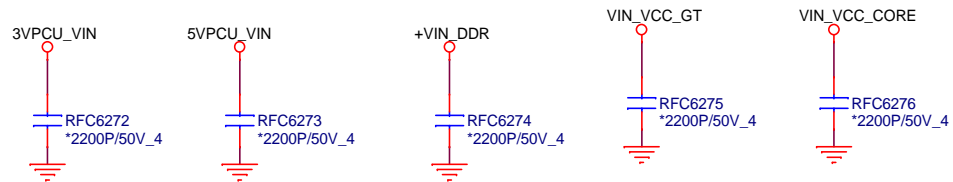
| | S3 | S5 | +1.35VSUS | REF | VTT |
|------------------|----|----|-----------|-----|-----|
| S0 | 1 | 1 | ON | ON | ON |
| S3 (main on off) | 0 | 1 | ON | ON | OFF |
| S4/S5 | 0 | 0 | OFF | OFF | OFF |







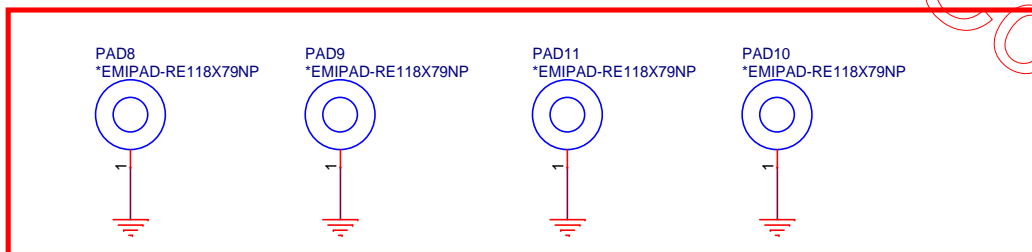




TOP

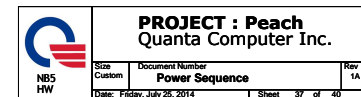


BOTTOM



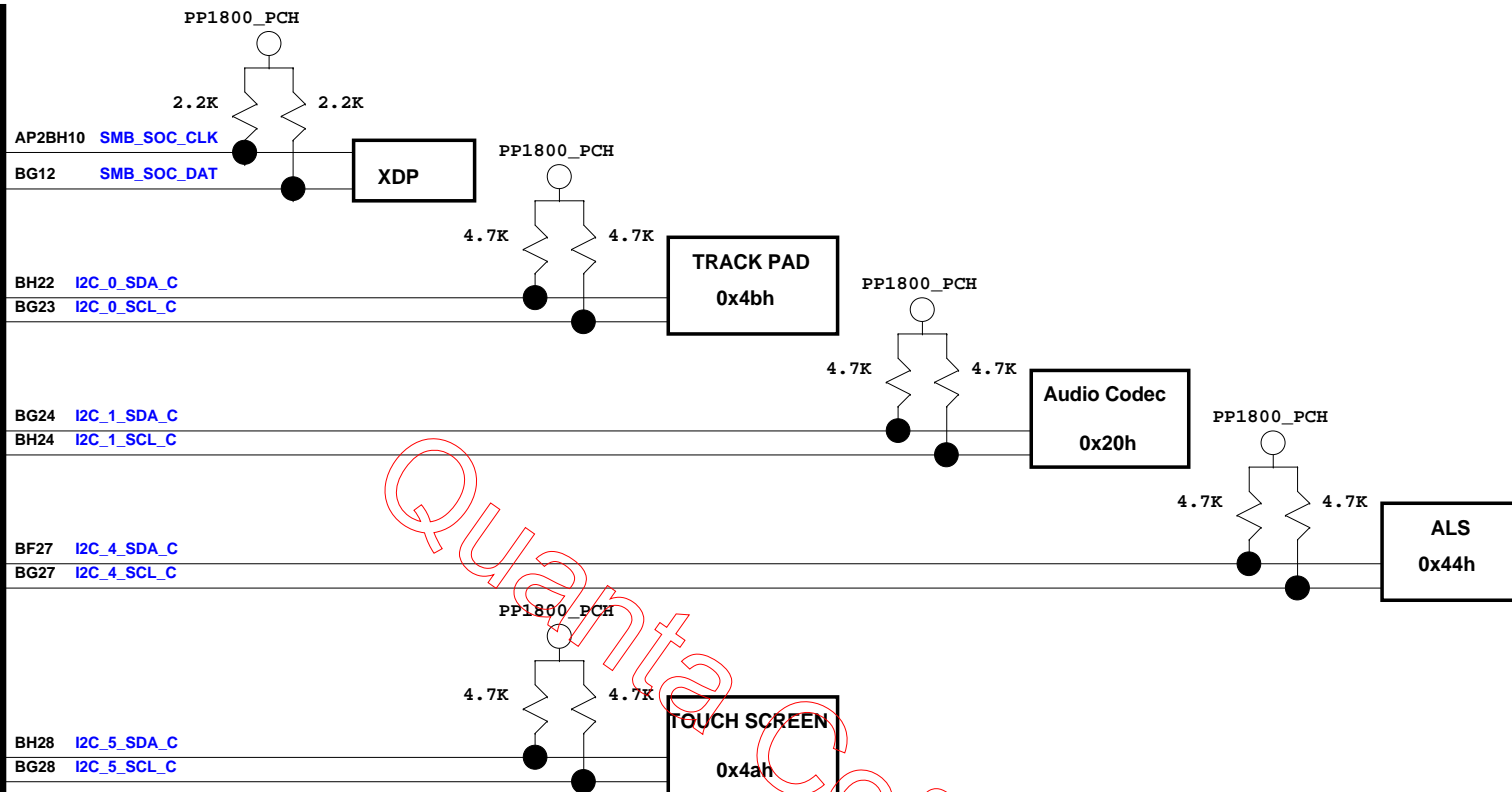
PROJECT : Peach
Quanta Computer Inc.

| | | |
|-----------------------------|---------------------------------|-----------|
| Size Custom | Document Number EM/RF | Rev 1A |
| Date: Friday, July 25, 2014 | Sheet 36 of 40 | |

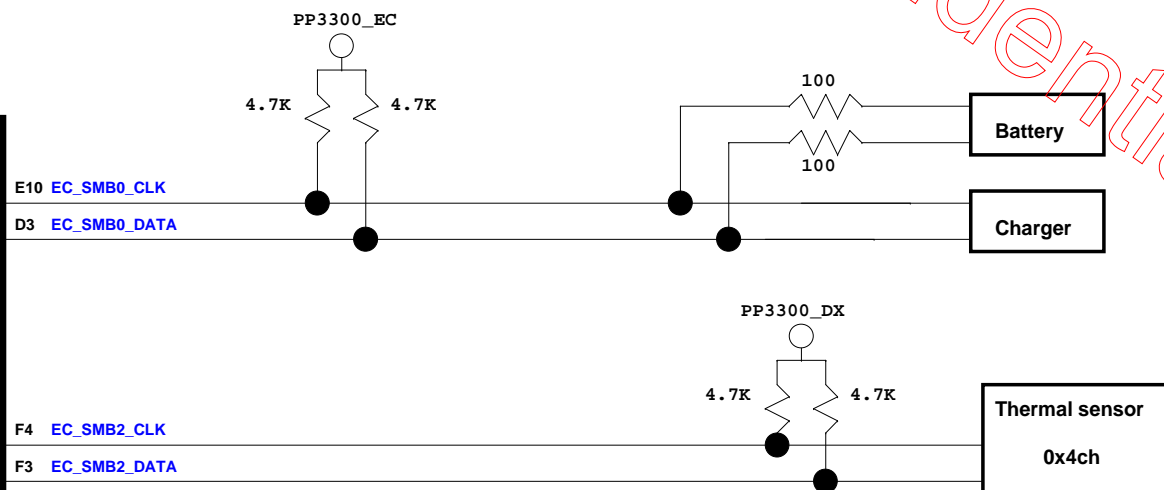


SMBUS
Bay-trail M

I2C

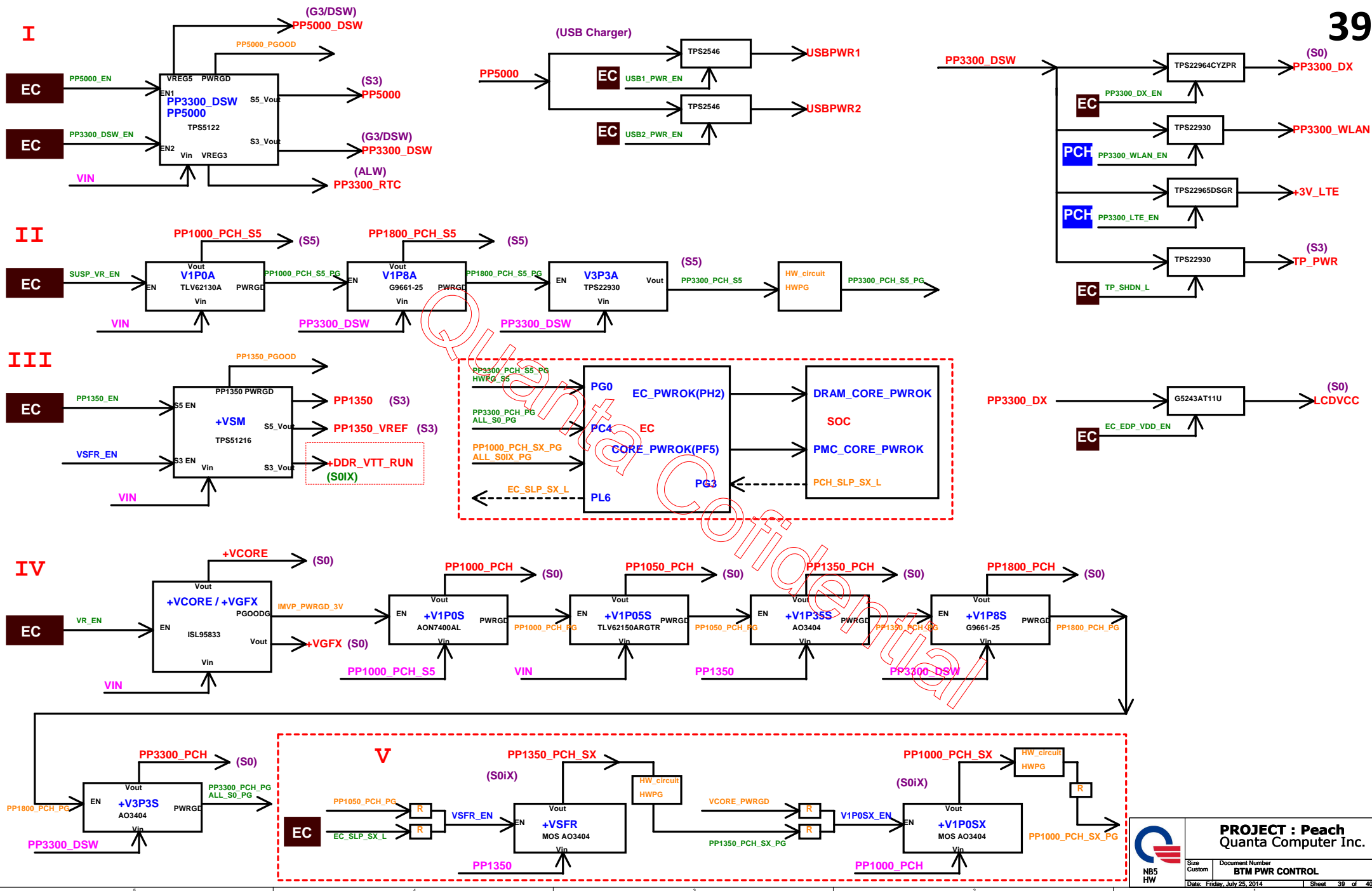



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